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EXAMINER
RYMAN, DANIEL J

ART UNIT	PAPER NUMBER
2665	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/462,895	CHITRE ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☒ Claim(s) *6 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.

2. The disclosure is objected to because of the following informalities: on page 8, line 12 "as listing" should be "as listed." On page 8, lines 13-14 "Satellite Receive (SR) 28" should be "Satellite Receive (SR) 30." On page 19, lines 20-21 "frame structure of Figure 3" should be "frame structure of Figure 5."

Appropriate correction is required.

Claim Objections

3. Claim 6 is objected to because of the following informalities: "is generating" should be "is generated." Appropriate correction is required.

4. Claim 27 is objected to because of the following informalities: "an ATM containing" should be "an ATM cell containing."

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 4 recites the limitation "said n number of ATM cells" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 5, 7, 8, 13, 19, 21, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iidaka et al (USPN 5,528,590) in view of Easki et al (USPN 5,440,547) in further view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770).

10. Regarding claims 1, 19, 21, 28, and 29, Iidaka discloses receiving an ATM cell stream comprised of a plurality of ATM cells (col. 2, lines 27-46); assembling a frame header made up of control and routing information for the plurality of ATM cells (col. 6, lines 4-10); assembling a payload frame made up of pay-loads of said number of said plurality of ATM cells (col. 6, lines 4-10). Iidaka possibly does not expressly disclose assembling a header frame made up of headers of a number of said plurality of ATM cells; however, Iidaka does disclose that the system must know how to convert between the destination address for a frame and the VCI information for the cells when the system converts between ATM cells and frames ("attaching a VPI/VCI conforming to the destination") (col. 6, lines 20-27). Rather than save this information in a routing table, which can be very costly, as is evidenced by Easki (col. 3, lines 35-42), it would have been obvious to one of ordinary skill in the art at the time of the invention to additionally transmit the header information in order to allow the system to determine the proper VCI/VPI information for each cell without relying on a costly routing table. Additionally, Iidaka in view

of Easki possibly does not expressly disclose detecting idle/unassigned cells within said cell stream and placing some of the detected idle/unassigned cells in a selected portion of the payload frame. It is very well known in ATM to use idle/unassigned cells for cell stuffing during rate adaptation and for filling bandwidth when there are no assigned cells to send. Naimpally discloses placing information in null data in order to take advantage of the otherwise wasted bandwidth (col. 4, lines 15-40). Wolf discloses detecting idle/unassigned cells so that control information can be placed within these cells (abstract and col. 2, lines 56-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to detect idle/unassigned cells so that the wasted bandwidth of these cells can be utilized. Wolf further discloses that it is important to keep the chronological sequence of the ATM cells in order to make "subsequent evaluations or tests easily possible" (col. 4, lines 8-20). It would have been obvious to one of ordinary skill in the art at the time of the invention to place some of the detected idle/unassigned cells in a selected portion of the payload frame in order to ensure that the chronological sequence of the cells is maintained, where the selected portion is broadly defined as the cell slot within the data stream which the null data is being used to fill. With respect to claim 28, Iidaka in view of Easki in further view of Naimpally in further view of Wolf suggests inserting error correction code into some of said idle/unassigned cells (Iidaka: col. 6, lines 4-8; Naimpally: col. 4, lines 15-40; and Wolf: abstract and col. 2, lines 56-58) in order to use the excess bandwidth to provide correction to protect against bit errors. While Iidaka in view of Easki in further view of Naimpally in further view of Wolf possibly does not expressly disclose setting a first information field within said frame at a first state when error correction code has been inserted into any idle/unassigned cells within said frame; and setting said first information field at a second state

when no error correction code has been inserted into idle/unassigned cells within said frame, such steps would have been obvious to one of ordinary skill in the art at the time of the invention in order to allow the receiver to properly process the received data stream.

11. Regarding claim 5, referring to claim 1, Iidaka in view of Easki in further view of Naimpally in further view of Wolf discloses that the step of assembling said header frame further comprises: adding a predetermined number of bytes of Header Error Correction Code (HECC) to said header frame (Iidaka: col. 5, lines 35-41 and col. 6, lines 4-8 and Easki: col. 3, lines 35-42).

12. Regarding claim 7, referring to claim 1, Iidaka in view of Easki in further view of Naimpally in further view of Wolf discloses that the step of placing idle/unassigned cells further comprises: adding Payload Error Correction Code in any idle/unassigned cells which are placed in said selected portion of said payload frame (Iidaka: col. 6, lines 4-8; Naimpally: col. 4, lines 15-40; and Wolf: abstract and col. 2, lines 56-58).

13. Regarding claim 8, referring to claim 1, Iidaka in view of Easki in further view of Naimpally in further view of Wolf discloses that assembling said payload frame further comprises: adding a predetermined number of bytes of Payload Error Correction Code (PECC) to said payload frame (Iidaka: col. 6, lines 4-8).

14. Regarding claim 13, Iidaka discloses encoding a plurality of ATM cells within an ATM cell stream, wherein said encoding step includes the steps of: assembling a frame header made up of control and routing information for the plurality of ATM cells (col. 6, lines 4-10), assembling a payload frame made up of pay-loads of said number of said plurality of ATM cells (col. 6, lines 4-10). Iidaka possibly does not expressly disclose assembling a header frame made up of headers of a number of said plurality of ATM cells; however, Iidaka does disclose that the system must

know how to convert between the destination address for a frame and the VCI information for the cells when the system converts between ATM cells and frames ("attaching a VPI/VCI conforming to the destination") (col. 6, lines 20-27). Rather than save this information in a routing table, which can be very costly, as is evidenced by Easki (col. 3, lines 35-42), it would have been obvious to one of ordinary skill in the art at the time of the invention to additionally transmit the header information in order to allow the system to determine the proper VCI/VPI information for each cell without relying on a costly routing table. Additionally, Iidaka in view of Easki possibly does not expressly disclose detecting idle/unassigned cells within said cell stream and placing some of the detected idle/unassigned cells in a selected portion of the payload frame. It is very well known in ATM to use idle/unassigned cells for cell stuffing during rate adaptation and for filling bandwidth when there are no assigned cells to send. Naimpally discloses placing information in null data in order to take advantage of the otherwise wasted bandwidth (col. 4, lines 15-40). Wolf discloses detecting idle/unassigned cells so that control information can be placed within these cells (abstract and col. 2, lines 56-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to detect idle/unassigned cells so that the wasted bandwidth of these cells can be utilized. It also would have been obvious to one of ordinary skill in the art at the time of the invention to place some of the detected idle/unassigned cells at the end of the payload and header frames in order to obtain a contiguous slot of bandwidth in which to insert information. Iidaka in view of Easki in further view of Naimpally in further view of Wolf further suggest adding Payload Error Correction Code in any idle/unassigned cells which are placed in said selected portion of said payload frame (Iidaka: col. 6, lines 4-8; Naimpally: col. 4, lines 15-40; and Wolf: abstract and col. 2, lines 56-58) in order to

use the excess bandwidth to ensure proper transmission of the data. Iidaka in view of Easki in further view of Naimpally in further view of Wolf possibly does not expressly disclose storing an idle/unassigned cell indicator in a first control byte in said header frame to be transmitted over said wireless link which indicates whether or not idle/unassigned cells have been placed at said selected portion of said payload frame; and storing a count of the number of idle/unassigned cells contained in the payload frame in a second control byte within said header frame; however, such steps would have been obvious to one of ordinary skill in the art. Iidaka in view of Easki in further view of Naimpally in further view of Wolf discloses storing extra information in the idle cells in order to take advantage of the excess bandwidth. A receiving device will not know which cells are idle cells and which cells are data cells. In order to ensure proper detection of the cells, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an indication that idle cells are present and the number of idle cells.

15. Claims 2, 3, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iidaka et al (USPN 5,528,590) in view of Easki et al (USPN 5,440,547) in further view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770) as applied to claims 1 and 21 above, and further in view of Yamashita (USPN 5,341,376).

16. Regarding claims 2, 3, and 22, referring to claims 1 and 21, Iidaka in view of Easki in further view of Naimpally in further view of Wolf possibly does not expressly disclose that the header frame is arranged in an i row x n column matrix or that the payload frame is arranged in an j row x m column matrix. Yamashita discloses using a matrix in order to organize the mapping of ATM cells into a frame format (abstract; Fig. 2; Fig. 3; Fig. 5; and col. 6, lines 48-57) where it is obvious that this is done in order to facilitate the mapping. It would have been

obvious to one of ordinary skill in the art at the time of the invention to use a matrix to facilitate the mapping of the ATM cells into a frame structure. Although Iidaka in view of Easki in further view of Naimpally in further view of Wolf does not expressly disclose that the matrix is an i row x n column matrix or an j row x m column matrix, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Yamashita discloses the use of a matrix, any size would have been obvious absent a showing of criticality by Applicant.

17. Regarding claim 23, referring to claim 22, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita discloses that assembling said payload frame further comprises: adding a predetermined number of bytes of Payload Error Correction Code (PECC) to said payload frame (Iidaka: col. 6, lines 4-8) where PECC is taken to be equivalent to frame error correction.

18. Claims 4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iidaka et al (USPN 5,528,590) in view of Easki et al (USPN 5,440,547) in further view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770) as applied to claims 1 and 19 above, and further in view of Jurkevich et al (USPN 5,282,207).

19. Regarding claims 4 and 20, referring to claims 1 and 19, Iidaka in view of Easki in further view of Naimpally in further view of Wolf possibly does not expressly disclose that said step of assembling said header frame further comprises: partitioning said header frame comprised of headers of an n number of ATM cells into a first section and a second section; said first section comprised of n - x number of headers of said n number of ATM cells and an added cell made up of control bytes, where the added cell of control bytes is broadly defined to be any header information; and said second section comprised of x number of headers of said n number of ATM cells. Jurkevich discloses partitioning a frame of data into a plurality of sections in order to group together traffic of the same type (abstract; col. 3, line 45-col. 4, line 9 and col. 4, lines 44-60). It would have been obvious to one of ordinary skill in the art at the time of the invention to partition the header frame into a first and second section in order to group together different types of traffic such that the similar types of traffic can be acted upon according to their requirements.

20. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iidaka et al (USPN 5,528,590) in view of Easki et al (USPN 5,440,547) in further view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770) as applied to claims 5 and 8 above, and further in view of Matsushita (USPN 5,608,738).

21. Regarding claims 6 and 9, referring to claims 5 and 8, Iidaka in view of Easki in further view of Naimpally in further view of Wolf possibly does not expressly disclose that the Header Error Correction Code or Payload Error Correction Code is generated using a Reed-Solomon coding scheme. Matsushita discloses that Reed-Solomon is a well-known coding scheme which provides error correction (col. 4, line 45-col. 5, line 62). It would have been obvious to one of

ordinary skill in the art at the time of the invention to use Reed Solomon coding since Reed-Solomon coding is a well-known error correction scheme.

22. Claims 10-12, 25-27, and 31-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iidaka et al (USPN 5,528,590) in view of Easki et al (USPN 5,440,547) in further view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770) in further view of Yamashita (USPN 5,341,376) in further view of Chitre et al (USPN 5,600,653).

23. Regarding claims 10, 25, 31, 32, and 33, Iidaka discloses receiving an ATM cell stream comprised of a plurality of ATM cells (col. 2, lines 27-46) where a wireline interface is a well known interface; encoding said plurality of ATM cells, wherein said encoding step includes the steps of: assembling a frame header made up of control and routing information for the plurality of ATM cells (col. 6, lines 4-10), assembling a payload frame made up of pay-loads of said number of said plurality of ATM cells (col. 6, lines 4-10). Iidaka possibly does not expressly disclose assembling a header frame made up of headers of a number of said plurality of ATM cells; however, Iidaka does disclose that the system must know how to convert between the destination address for a frame and the VCI information for the cells when the system converts between ATM cells and frames ("attaching a VPI/VCI conforming to the destination") (col. 6, lines 20-27). Rather than save this information in a routing table, which can be very costly, as is evidenced by Easki (col. 3, lines 35-42), it would have been obvious to one of ordinary skill in the art at the time of the invention to additionally transmit the header information in order to allow the system to determine the proper VCI/VPI information for each cell without relying on a costly routing table. Additionally, Iidaka in view of Easki possibly does not expressly disclose

detecting idle/unassigned cells within said cell stream and placing some of the detected idle/unassigned cells in a selected portion of the payload frame. It is very well known in ATM to use idle/unassigned cells for cell stuffing during rate adaptation and for filling bandwidth when there are no assigned cells to send. Naimpally discloses placing information in null data in order to take advantage of the otherwise wasted bandwidth (col. 4, lines 15-40). Wolf discloses detecting idle/unassigned cells so that control information can be placed within these cells (abstract and col. 2, lines 56-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to detect idle/unassigned cells so that the wasted bandwidth of these cells can be utilized. It also would have been obvious to one of ordinary skill in the art at the time of the invention to place some of the detected idle/unassigned cells at the end of the payload and header frames in order to obtain a contiguous slot of bandwidth in which to insert information. Iidaka in view of Easki in further view of Naimpally in further view of Wolf possibly does not expressly disclose that the header frame is arranged in an i row x n column matrix or that the payload frame is arranged in an j row x m column matrix. Yamashita discloses using a matrix in order to organize the mapping of ATM cells into a frame format (abstract; Fig. 2; Fig. 3; Fig. 5; and col. 6, lines 48-57) where it is obvious that this is done in order to facilitate the mapping. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a matrix to facilitate the mapping of the ATM cells into a frame structure. Although Iidaka in view of Easki in further view of Naimpally in further view of Wolf does not expressly disclose that the matrix is an i row x n column matrix or an j row x m column matrix, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular

recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Yamashita discloses the use of a matrix, any size would have been obvious absent a showing of criticality by Applicant. Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita possibly does not expressly disclose transmitting said predetermined number of said plurality of ATM cells over said wireless link by interleaving said header frame and said payload frame. Chitre discloses interleaving header and payload data in order to spread any bursty errors over the multiple original cells (abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to interleave the header and payload information in order to spread any bursty errors over the multiple original cells. In addition, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre discloses reversing the processes of encoding and interleaving in order to obtain the original cell stream at the receiver, where it is well known in the art for a receiver to lock onto a predetermined synchronization pattern in order to properly receive and interpret the received cell stream.

24. Regarding claim 11, referring to claim 10, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre discloses interleaving by transmitting a third predetermined number of bytes from said payload

frame for every byte transmitted from said header frame (Chitre: abstract and col. 1, line 66-col. 2, line 38).

25. Regarding claim 12, referring to claim 10, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre discloses adding a synchronizing pattern to said header and payload frames (Yamashita: col. 4, lines 54-60), where from reasoning similar to that used in the rejections of claims 2 and 3, it would be obvious to use a two byte synchronizing pattern.

26. Regarding claim 26, referring to claim 25, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre suggests that the step of placing idle/unassigned cells further comprises: adding Payload Error Correction Code in any idle/unassigned cells which are placed in said selected portion of said payload frame (Iidaka: col. 6, lines 4-8; Naimpally: col. 4, lines 15-40; and Wolf: abstract and col. 2, lines 56-58).

27. Regarding claim 27, referring to claim 25, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre discloses generating a header syndrome (HEC) (Iidaka: col. 5, lines 31-40). Although Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre possibly does not expressly disclose identifying bits in error using said header syndrome; wherein when a single bit in error is identified in the header, correction of said bit in error is performed, and when multiple bits in error are identified in the header, an ATM cell containing said multiple bits in error is dropped and replaced by an idle/unassigned cell, such steps are well known in the art. It would have been obvious to one of ordinary skill in the art at

the time of the invention to use the syndrome to detect and correct bit errors in order to ensure proper transmission. It also would have been obvious to one of ordinary skill in the art at the time of the invention to drop cells containing multiple bit errors and thus cannot be corrected with idle/unassigned cells being used to fill in the extra bandwidth.

28. Regarding claims 34, 36, and 37, incorporating rejections of claims 10, 11, 12, 25, 31, 32, and 33, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre possibly does not further expressly disclose declaring a synchronization mode when the number of bytes in error between successive synchronization patterns is less than a predetermined number; however, it is well known in the art to declare synchronization when the number of bytes in error between successive synchronization patterns is less than a predetermined number. When synchronizing, a receiver searches for a known pattern. If the pattern is not found, then a comparison of synchronization patterns will not yield a match. Conversely, if the pattern is found, then a comparison will yield a match except for random bit errors in the pattern due to interference during transmission. For these reasons, it would have been obvious to one of ordinary skill in the art at the time of the invention to declare synchronization when the number of bytes in error between successive synchronization patterns is less than a predetermined number.

29. Regarding claim 35, referring to claim 34, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre possibly does not expressly disclose that said step of detecting includes setting a pattern search window of a predetermined number of bytes; however, using a pattern search window is well known in order to detect the predetermined number of bytes of the pattern.

30. Regarding claim 38, incorporating rejections of claims 10, 11, 12, 25, 31, 32, and 33, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre possibly does not expressly further disclose detecting if any cells within a Header frame within said predetermined frame are uncorrectable; and replacing detected uncorrectable cells with idle/unassigned cells; however, such steps are well known in the art as a way to eliminate corrupted data from the system, thereby, eliminating the need to further process data that is not usable.

31. Regarding claim 39, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita in further view of Chitre suggests checking control bytes contained with said Header frame to determine whether or not idle/unassigned cells were utilized for error correction in a Payload Frame within said predetermined frame (Naimpally: col. 4, lines 15-40 and Wolf: abstract and col. 2, lines 56-58); reading a plurality of header bytes within said Header frame and forming a table of sequence numbers based upon said read header bytes and reinserting idle/unassigned cells into said correct positions in said predetermined frame based upon said table of sequence numbers thereby restoring an order of cells occurring at a transmitting end of said wireless link (Wolf: col. 4, lines 8-20) where sequence numbers are well known in the art as a means to determine the correct position of a cell relative to other cells.

32. Claims 14 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagaki et al (USPN 5,657,316) in view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770).

33. Regarding claims 14 and 30, Nakagaki discloses a method for recording information to be used at a receiving end of an ATM wireless link relating to original positions of moved

idle/unassigned cells in an ATM frame, comprising: recording original positions (sequence numbers) of idle/unassigned cells as they occur in a cell stream made up of a predetermined number of ATM cells used to assemble said ATM frame having a header frame and a payload frame (col. 5, lines 1-23) and restoring said original positions of said idle/unassigned cells within said cell stream based upon said recorded original positions after transmission of said frame over said wireless link (abstract; col. 2, lines 64-67; and col. 3, lines 8-24). Nakagaki possibly does not expressly disclose moving idle/unassigned cells to new positions at a selected portion of said ATM frame. It is very well known in ATM to use idle/unassigned cells for cell stuffing during rate adaptation and for filling bandwidth when there are no assigned cells to send. Naimpally discloses placing information in null data in order to take advantage of the otherwise wasted bandwidth (col. 4, lines 15-40). Wolf discloses detecting idle/unassigned cells so that control information can be placed within these cells (abstract and col. 2, lines 56-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to detect idle/unassigned cells so that the wasted bandwidth of these cells can be utilized. It also would have been obvious to one of ordinary skill in the art at the time of the invention to place some of the detected idle/unassigned cells at the end of the payload and header frames in order to obtain a contiguous slot of bandwidth in which to insert information. Nakagaki in view of Naimpally in further view of Wolf possibly does not expressly disclose overwriting header bytes of each moved idle/unassigned cell with the recorded original positions of each corresponding moved idle/unassigned cell (sequence numbers) since Nakagaki in view of Naimpally in further view of Wolf discloses that the sequence numbers are added to the payload (Nakagaki: Fig. 6D and 6E). Writing the sequence number of the idle/unassigned cell in the header of the cell would have

been obvious to one of ordinary skill in the art at the time of the invention in order to allow the entire bandwidth of the payload to be used for the insertion of new data. It would have been obvious to one of ordinary skill in the art at the time of the invention to write the sequence number in the header of the idle/unassigned cell in order to have a larger slot of unused contiguous bandwidth that can be utilized in the idle/unassigned cell.

34. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shobatake et al (USPN 5,557,609).

35. Regarding claim 15, Shobatake discloses receiving a plurality of ATM cells each having a header and a payload, where it is obvious that each ATM cell contains a header and payload, said header including at least one Header Error Correction byte (col. 5, lines 41-col. 6, line 3); dropping said at least one Header Error Correction byte from said header of each ATM cell to thereby leave an unoccupied byte space in said header (col. 6, lines 4-9); inserting other information into said unoccupied byte space (col. 6, lines 4-9) where the other information is the new HEC value; and transmitting each of said plurality of ATM cells (col. 6, lines 10-16).

36. Regarding claim 16, referring to claim 15, Shobatake discloses regenerating said Header Error Correction byte from the remaining bytes in said header of each ATM cell after transmission of each cell (col. 6, lines 4-9) where it is obvious that this regeneration could occur an additional time after the ATM cell has been transmitted.

37. Regarding claim 17, referring to claim 15, Shobatake discloses generating a header syndrome (col. 6, lines 4-9) where the syndrome is broadly defined as the HEC. Shobatake possibly does not expressly disclose identifying bits in error using said header syndrome; wherein when a single bit in error is identified in the header, correction of said bit in error is

performed, and when multiple bits in error are identified in the header, an ATM cell containing said multiple bits in error is dropped and replaced by an idle/unassigned cell; however, such steps are well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the syndrome to detect and correct bit errors in order to ensure proper transmission. It also would have been obvious to one of ordinary skill in the art at the time of the invention to drop cells containing multiple bit errors and thus cannot be corrected with idle/unassigned cells being used to fill in the extra bandwidth.

38. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagaki et al (USPN 5,657,316).

39. Regarding claim 18, Nakagaki discloses a method for preserving overhead parity bits present in each of a plurality of received ATM frames which are to be transmitted over a wireless link comprising: flagging a section occurring in each of said plurality of ATM frames received (add sequence number) (col. 3, lines 7-24 and col. 5, lines 1-8) where it would be obvious to flag the first nibble in order to ensure that the sequence number is one of the first pieces of information read when receiving an ATM frame; assembling header and payload frames for transmission over said wireless link consisting of a predetermined number of ATM cells derived from said plurality of ATM frames (abstract; col. 4, line 30-col. 5, line 23; col. 5, line 61-col. 7, line 43; col. 8, line 26-col. 10, line 14; and col. 11, lines 23-41); recording a position of each said first flagged nibble encountered in each said predetermined number of ATM cells in control bytes contained in said header frame (sequence numbers) (col. 3, lines 7-24 and col. 5, lines 1-8); and storing said overhead parity bits occurring in each of said plurality of ATM frames in control

bytes contained in said header frame (col. 4, line 30-col. 5, line 23; col. 5, line 61-col. 7, line 43; col. 8, line 26-col. 10, line 14; and col. 11, lines 23-41).

40. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iidaka et al (USPN 5,528,590) in view of Easki et al (USPN 5,440,547) in further view of Naimpally et al (USPN 5,650,825) in further view of Wolf et al (USPN 5,892,770) in further view of Yamashita (USPN 5,341,376) as applied to claim 23 above, and further in view of Matsushita (USPN 5,608,738).

41. Regarding claim 24, referring to claim 23, Iidaka in view of Easki in further view of Naimpally in further view of Wolf in further view of Yamashita possibly does not expressly disclose that the Payload Error Correction Code is generated using a Reed-Solomon coding scheme. Matsushita discloses that Reed-Solomon is a well-known coding scheme which provides error correction (col. 4, line 45-col. 5, line 62). It would have been obvious to one of ordinary skill in the art at the time of the invention to use Reed Solomon coding since Reed-Solomon coding is a well-known error correction scheme.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (703)305-6970. The examiner can normally be reached on Mon.-Fri. 7:00-5:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703)308-6602. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-6743 for regular communications and (703)308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Daniel J. Ryman
Examiner
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